THE INVENTION CLAIMED IS:

1. A method of manufacturing an integrated circuit comprising:
processing a substrate to form a core opening and an isolation opening;
depositing an insulating material in the core opening and the isolation opening;
forming a core mask over the isolation opening;
removing the insulating material in the core opening using the core mask;
removing the core mask;
depositing a doped bitline material over the core opening and the isolation opening;
planarizing the doped bitline material; and
thermal annealing the doped bitline material to form a high conductivity bitline.

2. The method of manufacturing an integrated circuit as claimed in claim 1 wherein:
depositing the doped bitline material deposits a doped polysilicon; and
thermal annealing causes dopant diffusion into the substrate to form the high conductivity bitline.

3. The method of manufacturing an integrated circuit as claimed in claim 1 wherein the insulating material is selected from a group consisting of oxides and nitrides.

4. The method of manufacturing an integrated circuit as claimed in claim 1 wherein planarizing the doped bitline material planarizes the insulating material over the isolation opening to form an isolation region.

5. The method of manufacturing an integrated circuit as claimed in claim 1 wherein:
processing the substrate includes forming a core region and a peripheral region; and
forming the core mask covers the peripheral region and exposes the core region.

6. The method of manufacturing an integrated circuit as claimed in claim 1 wherein processing the substrate includes:
depositing a hard mask layer on the substrate;
depositing a photoresist on the hard mask layer;
processing the photoresist and the hard mask layer to form a hard mask; and
using the hard mask to form the core opening and the isolation opening.

7. The method of manufacturing an integrated circuit as claimed in claim 1 including:

depositing a charge-trapping layer over the high conductivity bitline and the substrate;

depositing a wordline layer over the charge-trapping layer; and

forming a wordline over and perpendicular to the high conductivity bitline.

8. A method of manufacturing an integrated circuit comprising:

providing a semiconductor substrate;

processing the semiconductor substrate to form a core trench and a shallow trench isolation (STI) trench;

depositing an insulating material in the core trench and the STI trench;

depositing a photoresist over the core trench and the STI trench;

processing the photoresist to form a core mask over the STI trench;

removing the insulating material in the core trench using the core mask;

removing the core mask;

depositing a doped bitline material over the core trench and the STI trench;

planarizing the doped bitline material and the insulating material; and

thermal annealing the doped bitline material to form a high conductivity bitline.

9. The method of manufacturing an integrated circuit as claimed in claim 8 wherein:

depositing the doped bitline material deposits a doped polysilicon; and

thermal annealing causes dopant diffusion from the doped bitline material into the semiconductor substrate to form the high conductivity bitline.

10. The method of manufacturing an integrated circuit as claimed in claim 8 wherein the insulating material is selected from a group consisting of oxides and nitrides.

11. The method of manufacturing an integrated circuit as claimed in claim 8 wherein planarizing the doped bitline material simultaneously planarizes the insulating material over the STI trench to form a STI.

12. The method of manufacturing an integrated circuit as claimed in claim 8 wherein:

processing the substrate includes forming a core region and a peripheral region separated by the STI trench; and

processing the photoresist to form the core mask covers the peripheral region and exposes the core region, the core mask also covers the insulating material in the STI trench.

13. The method of manufacturing an integrated circuit as claimed in claim 8 wherein processing the substrate includes:

depositing a hard mask layer on the substrate;

depositing an anti-reflective coating on the hard mask layer;

depositing a further photoresist on the anti-reflective coating;

processing the further photoresist, the anti-reflective coating, and the hard mask layer to form a hard mask; and

using the hard mask to form the core trench and shallow trench isolation trench.

14. The method of manufacturing an integrated circuit as claimed in claim 8 including:

depositing a charge-trapping layer over the high conductivity bitline;

depositing a wordline layer over the charge-trapping layer;

processing an additional photoresist layer, an additional anti-reflective coating layer, and a hard mask layer to form a patterned photoresist and patterned anti-reflective coating;

using the patterned photoresist and patterned anti-reflective coating to form a hard mask; and

using the hard mask to form a wordline over and perpendicular to the high conductivity bitline.

15. A method of manufacturing a Flash memory integrated circuit comprising:

providing a semiconductor substrate;

processing the semiconductor substrate to form a plurality core trenches parallel and spaced apart and a plurality of shallow trench isolation (STI) trenches enclosing portions of the semiconductor substrate;

depositing an insulating material over and in the core trench and the STI trench;

depositing a photoresist over the semiconductor substrate, the plurality of core trenches, and the plurality of STI trenches;

processing the photoresist to form a core mask over a portion of the semiconductor substrate and the plurality of STI trenches;

removing the insulating material in the plurality of core trenches using the core mask;

removing the core mask;

depositing a doped bitline material in the plurality of core trenches and the plurality of STI trenches;

planarizing the doped bitline material and the insulating material; and

thermal annealing the doped bitline material to form a plurality of high conductivity bitlines.

16. The method of manufacturing a Flash memory integrated circuit as claimed in claim 15 wherein:

providing the semiconductor substrate provides a p-doped semiconductor substrate;

depositing the doped bitline material deposits a n-doped polysilicon; and

thermal annealing causes n-dopant from the doped bitline material into the semiconductor substrate to form the plurality of high conductivity bitlines.

17. The method of manufacturing a Flash memory integrated circuit as claimed in claim 15 wherein the insulating material is selected from a group consisting of oxides and nitrides.

18. The method of manufacturing a Flash memory integrated circuit as claimed in claim 15 wherein planarizing the doped bitline material and the insulating material on the semiconductor substrate using chemical mechanical polishing simultaneously forms a plurality of bitlines and a plurality of STIs.

19. The method of manufacturing a Flash memory integrated circuit as claimed in claim 15 wherein:

processing the semiconductor substrate includes forming a core region and a peripheral region separated by at least one of the plurality of STI trenches; and

processing the photoresist to form the core mask covers the peripheral region and exposes the core region, the core mask also covers the insulating material in the STI trench.

20. The method of manufacturing a Flash memory integrated circuit as claimed in claim 15 wherein processing the substrate includes:

depositing a hard mask layer on the semiconductor substrate;

depositing an anti-reflective coating on the hard mask layer;

depositing a further photoresist on the anti-reflective coating;

processing the further photoresist, the anti-reflective coating, and the hard mask layer to form a hard mask;

removing the further photoresist and the anti-reflective coating;

using the hard mask to form the core trench and shallow trench isolation trench; and

removing the hard mask.

21. The method of manufacturing a Flash memory integrated circuit as claimed in claim 15 including:

depositing a charge-trapping layer over the plurality of high conductivity bitlines;

depositing a wordline layer over the charge-trapping layer;

processing an additional photoresist layer, an additional anti-reflective coating layer, and a hard mask layer to form a patterned photoresist and patterned anti-reflective coating;

using the patterned photoresist and patterned anti-reflective coating to form a hard mask; and

using the hard mask to form a plurality of wordlines over and perpendicular to the plurality of high conductivity bitlines.